REMARKS

Claims 1-10 and 12-15 are pending in this application. By this Amendment, Applicants amend claims 1-5, 9 and 15.

Claims 2-10 were rejected under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite. Claim 2 has been amended to properly depend upon claim 13 to provide proper antecedent basis for "the doped layer". Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 1, 2, 4, 6, 8-10 and 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sawada et al. ("A Super Low-Noise AlGaAs/InGaAs/GaAs DC-HFET with 0.15 micron Gate-Length"). Claims 3, 5 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sawada et al. And claims 12-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sawada et al. in view of Inai et al. ("Doped Channel HFET with Effective Lateral Energy Modulation for High Power Enhancement Operation"). Applicants respectfully traverse these rejections.

Claim 1 has been amended to recite:

> "A field-effect semiconductor device comprising:
> a channel layer;
> a contact layer;
> a semiconductor structure having an electron-affinity different from those of the channel layer and the contact layer and formed between the channel layer and the contact layer, the semiconductor structure having a first junction face between the semiconductor structure and the channel layer and having a second junction face between the semiconductor structure and the contact layer;
> an ohmic electrode formed on the contact layer; and
> a Schottky electrode formed on the semiconductor structure;
> wherein **both of the first junction face and the second junction face are iso-type heterojunctions**; and
> **the semiconductor structure is composed of a single material and includes at least two semiconductor layers.**" (Emphasis added)

Claim 15 has been amended to recite:

> "A field-effect semiconductor device comprising:
> a channel layer;
> a contact lay r;
> a semiconductor structure having an electron-affinity different from those of the channel layer and the contact layer, **the s miconductor**

structure having at least two layers;
an ohmic electrode formed on the contact layer; and
a Schottky electrode formed on the semiconductor structure;
wherein
the semiconductor structure is formed between the channel layer and the contact layer, and **where a junction between said layers of the semiconductor device is a heterojunction, the junction is an iso-type heterojunction**." (Emphasis added)

The Examiner alleged that Sawada et al. teaches all of the features recited in claims 1 and 15 of the present application including a doped n-InGaAs channel layer; a doped barrier layer (or semiconductor structure) composed of n-AlGaAs, and a doped contact layer composed of n-GaAs.

However, the barrier layer (or semiconductor structure) of Sawada et al. is composed of only a **single** layer, **NOT** of at least two layers as recited in claims 1 and 15 of the present application. Thus, Sawada et al. clearly fails to teach or suggest "the semiconductor structure is composed of a single material and includes at least two semiconductor layers" or "the semiconductor structure having at least two layers" and as recited in the present claimed invention.

Inai et al. teaches a device in which every heterojunction provided therein is an **aniso-type** heterojunction, such as i-AlGaAs/n-GaAs. Inai et al. fails to teach or suggest **any iso-type** heterojunctions, and certainly fails to teach or suggest "both of the first junction face and the second junction face are iso-type heterojunctions" as recited in claim 1 of the present application.

Furthermore, since each and every one of the heterojunctions in Inai et al. ~~are~~is an **aniso-type** heterojunction, Inai et al. clearly fails to teach or suggest "where a junction between said layers of the semiconductor device is a heterojunction, the junction is an iso-type heterojunction" as recited in claim 15 of the present application.

In the Response to Arguments section of the outstanding Office Action, the Examiner acknowledged that "Inai et al. does not anticipate the claims, but has taken the position that it would have been obvious to substitute n-AlGaAs for the n-GaAs barrier layer of Inai." In support of the Examiner's position, the Examiner alleged that it would have been obvious to hav "modified the Sawada n-AlGaAs barrier layer by

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providing an additional undoped layer between the top and bottom portions . . . for the purpose of achieving a larger breakdown voltage with the undoped insulating AlGaAs layer while simultaneously reducing the barrier-contact band-discontinuities/resistance as taught by Inai." This is clearly incorrect.

Section 2 of Inai et al., clearly and specifically discloses that "the n-AlGaAs intermediate layer", **NOT** the "undoped AlGaAs layer," achieves the advantages upon which the Examiner has relied to allegedly provide motivation to combine the teachings of Inai et al. with Sawada et al. Particularly, Inai et al. discloses "the intermediate layer plays a role of achieving both large breakdown voltage and low series resistance. Moreover, it prevents the effect of surface depletion layer between the gate and the source or the drain." As clearly seen in Fig. 1 of Inai et al., the **doped** n-AlGaAs intermediate layer is disposed directly adjacent to the n/n' GaAs contact layer, **NOT** between two layers of the semiconductor structure (barrier layer).

Thus, there would have clearly been **no** motivation to combine or modify the semiconductor structure of Sawada et al. to include the undoped AlGaAs layer of Inai et al. as alleged by the Examiner. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In re Geiger, 815 F.2d 686, 2 USPQ 1276, 1278 (Fed. Cir. 1987).

Instead of basing the conclusion of obviousness on actual teachings or suggestions of the prior art and the knowledge of one of ordinary skill in the art at the time the invention was made, the Examiner has improperly used Applicants' own invention as a guide. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. In re Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992).

In fact, Inai et al. clearly and specifically teaches away from providing an undop d AlGaAs layer without the dop d n-AlGaAs intermediate layer. Particularly, Inai

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et al. discloses that "an undoped barrier layer commonly buried under the base electrode inevitably causes large channel series resistance. This series resistance degrades DC characteristics such as transconductance, drain conductance and knee voltage, resulting in poor output power characteristics." Accordingly, Inai et al. cannot be relied upon in an obviousness rejection of Applicants' claimed invention since it is error to find obviousness where references diverge and teach away from the invention at hand. W.L. Gore & Assoc. v. Garlock Inc., 721 F .2d 1540, 1550, 220 USPQ 303, 311 (Fed. Cir. 1983).

Alternatively, the Examiner alleged that it would have been obvious to have "modified Inai's barrier structure by substituting a doped AlGaAs barrier for the doped GaAs barrier that is adjacent to the n-InGaAs channel, as taught by Sawada, for the purpose of better reducing the gate leakage and increasing the barrier/channel junction conduction-band discontinuity for better carrier confinement in the channel." Applicants respectfully disagree.

Sawada et al. teaches only a **single** barrier layer. Thus, there would have been absolutely **no** motivation to substitute a doped AlGaAs barrier of Sawada et al. for the doped GaAs barrier of Inai et al. (which is one of three barrier layers), since the combination and arrangement of layers in Sawada et al. is completely different from the combination and arrangement of layers of Inai et al. In addition, Sawada et al. neither teaches nor suggests that the AlGaAs barrier layer could or should be used in combination with additional barrier layers, as alleged by the Examiner. Furthermore, there is absolutely no teaching or suggestion in Inai et al. that the GaAs layer could or should be substituted with an AlGaAs layer as alleged by the Examiner.

Furthermore, since a heterojunction exists between the undoped AlGaAs layer and the GaAs layer of Inai et al. which is clearly **not** an iso-type heterojunction, Inai et al. certainly fails to teach or suggest "where a junction between said layers of the semiconductor device is a heterojunction, th junction is an iso-typ heterojunction" as recited in claim 15 of the present application.

Accordingly, Applicants respectfully submit that Sawada et al. and Inai et al., applied alone or in combination, fail to t ach or suggest the uniqu combination and

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arrangement of elements recited in claims 1 and 15 of the present application.

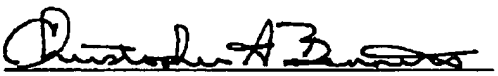
In view of the foregoing remarks, Applicants respectfully submit that claims 1 and 15 are allowable. Claims 2-10 and 12-14 depend upon claim 1, and are therefore allowable for at least the reasons that claim 1 is allowable.

In view of the foregoing Remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: April 7, 2003



Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080

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